# Nonvolatile Memory Technologies: A Look into the Future

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# Key Messages

- Moore's Law will continue through innovation
  - Process complexity will increase to address fundamental limits of physics
- To maintain Moore's Law cost learning curve, difficult to do it by transistor technology alone
  - New opportunity for new memory structures and new materials
- Current mainstream memory technologies of ETOX and NAND will continue to be the key technologies for more than 5 years out
- Intense research activities to identify scalable memory technologies for 5 year and beyond

# Agenda

- **Moore's Law will continue**
- **Emerging new memory technologies**
- **Market Potential for new memory technologies**
- **Comparison of three memory technologies**
- **Development Considerations**
- **Summary**

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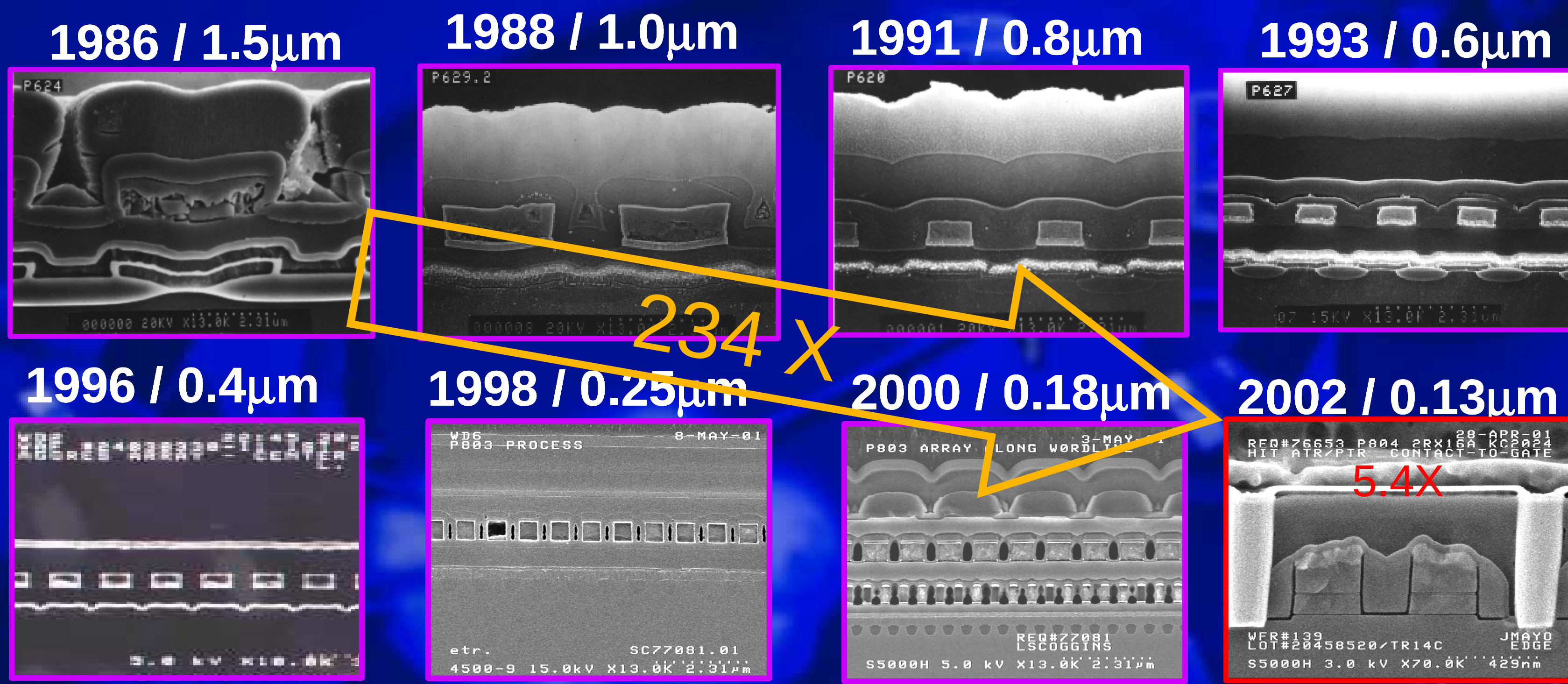
# Moore's Law will Continue with ETOX® Flash

- Currently shipping 8th generation of ETOX® flash memory in high volume
  - ~50% cell size reduction per generation
- Good visibility into 90 nm and 65 nm generation
- Current projection shows scaling continues at 45 nm node but challenged to meet 50% goal
- Further innovation required to maintain cost learning curve
- Industry trend: complex transistor structure to meet scaling challenges

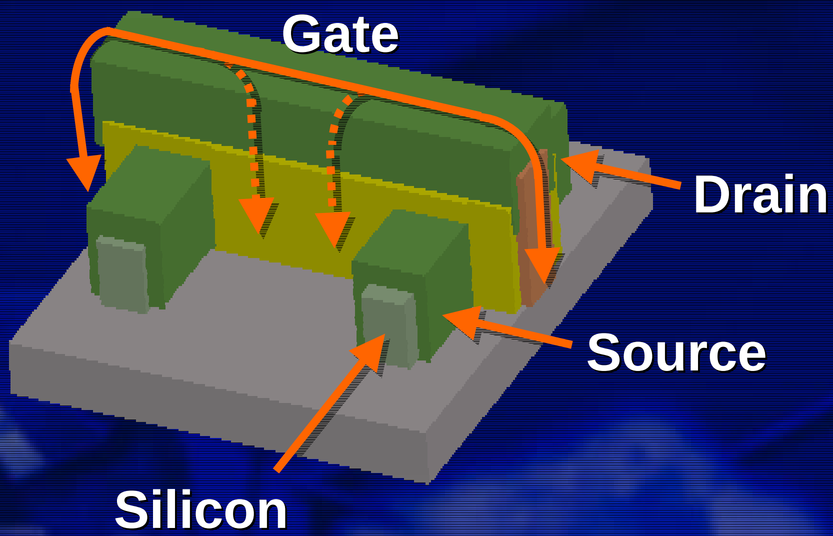
# ETOX® Technology Scaling

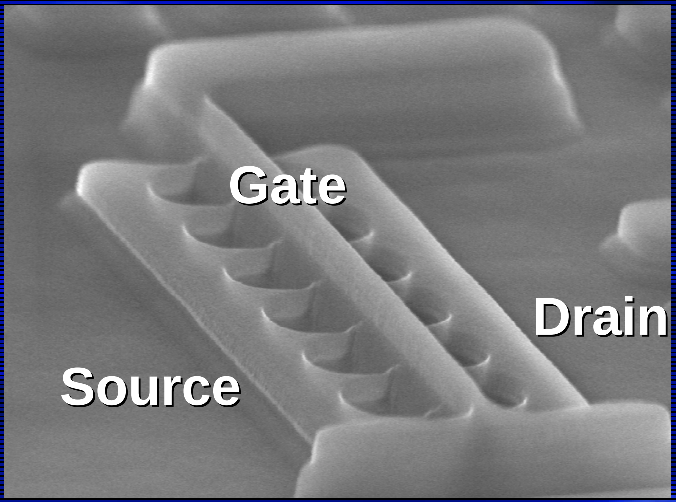



Volume Production Year / Technology Generation

- **18 years and 8 Generations of ETOX® to 0.13 µm**

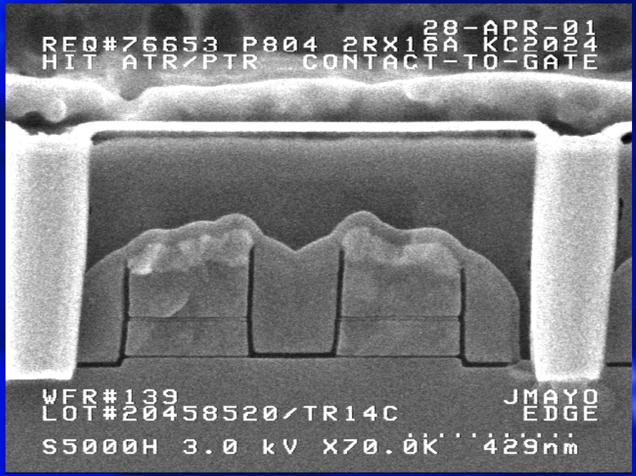
# Example of Future Transistor




Source: Intel

# Example of Current Flash Memory Cell



# New Materials in Silicon Technology

- The semiconductor industry has been addressing the performance and cost issues by introducing new materials
  - Tantalum pentoxide for DRAM storage dielectric
  - Cobalt and Nickel for S/D formation
  - Copper and low k dielectric for interconnect
  - High K dielectric for transistor gate
- For non-volatile memories, new memory materials provide new opportunities for further memory cost reduction

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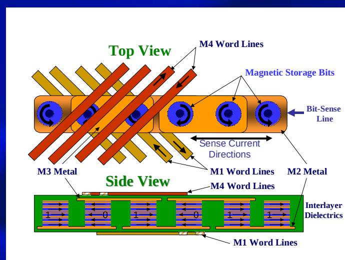
# NV Memory Mechanisms

| Transistor Vt Shifts | Charge Displacement | Resistance Change |
|---|---|---|
| 1. Floating gate<br>2. Floating Trap (nitride) | 1. Crystalline Ferroelectric<br>2. Polymer Ferroelectric | 1. Magnetic: GMR or MJT<br>2. Phase Change<br>3. Complex metal oxide<br>4. Polymer ionic transport |

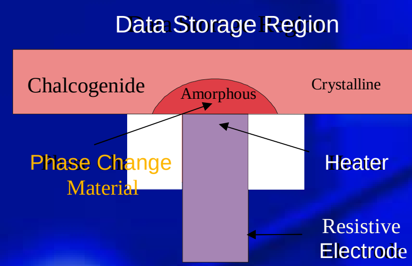
**All involve new material**

# Emerging Non-Volatile Memories

## MRAM

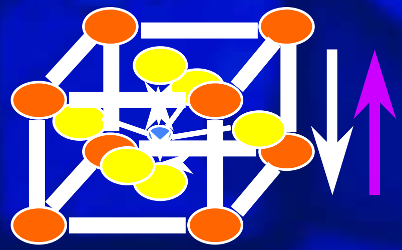



## OUM

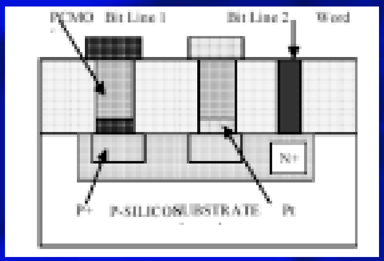



## Polymer

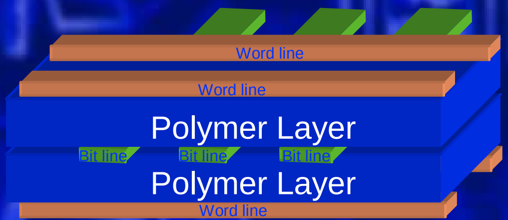

## FERAM



## RRAM

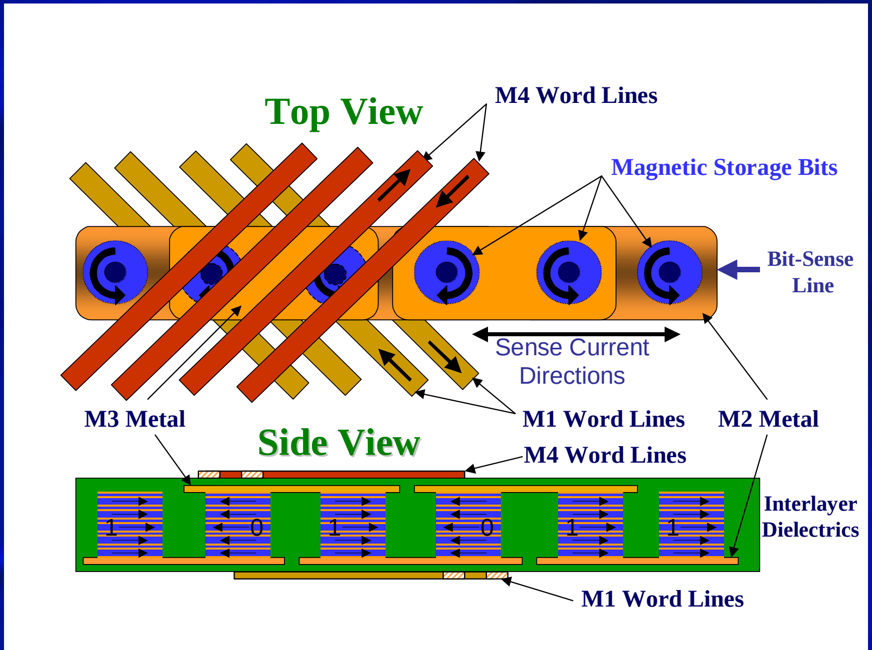


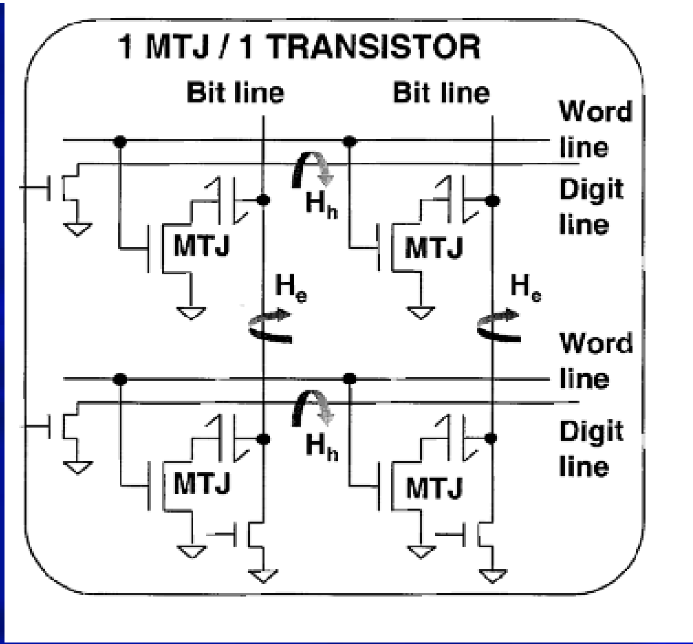

## FE Polymer



# What Is MRAM?

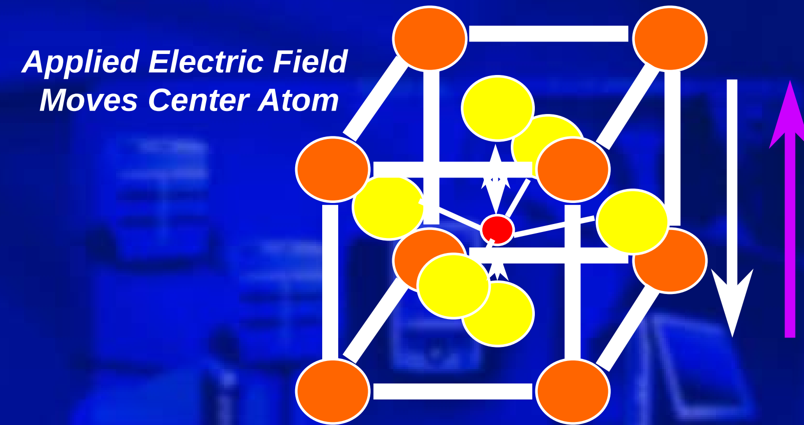
- Operation
  - Cell is 1 MJT + 1 Transistor
  - Electric current switches the magnetic polarity
  - Change in magnetic polarity sensed as resistance change
- Attributes
  - Non-Volatile
  - High Density
  - Non Destructive Read
  - Low Voltage & Low Power
  - Write = Read Speed, < 50 nsec
  - Unlimited R/W Endurance
  - Material compatibility with CMOS a key challenge



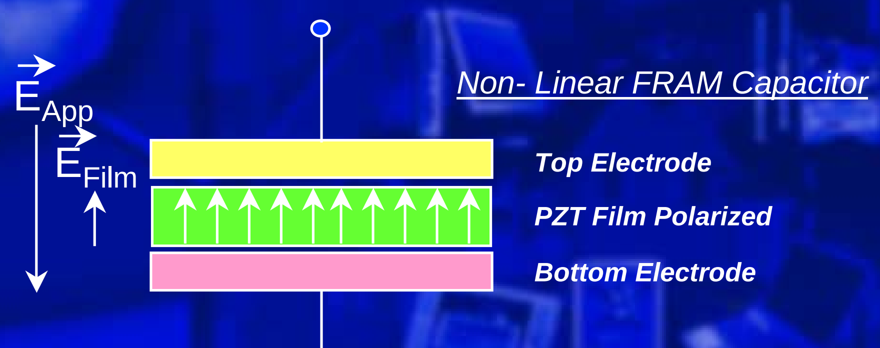
# What Is FeRAM?

- **Operation**
  - **Selected PZT crystalline materials have bi-stable center atom**
  - **Data is stored by applying an voltage to polarize the internal dipoles “Up” or “Down”**
  - **Non-Linear FRAM Read Capacitor**
- **Attributes**
  - **Non-Volatile**
  - **Larger Cell Size**
  - **“Fast” Random Read Access**
  - **Fast Write with very low power consumption**
  - **Destructive read, limited read and write cycles**




Perovskite Crystal Unit Cell
PZT (PbO,$ZrO_2$, $TiO_2$) Lead-Zirconate-Titanate

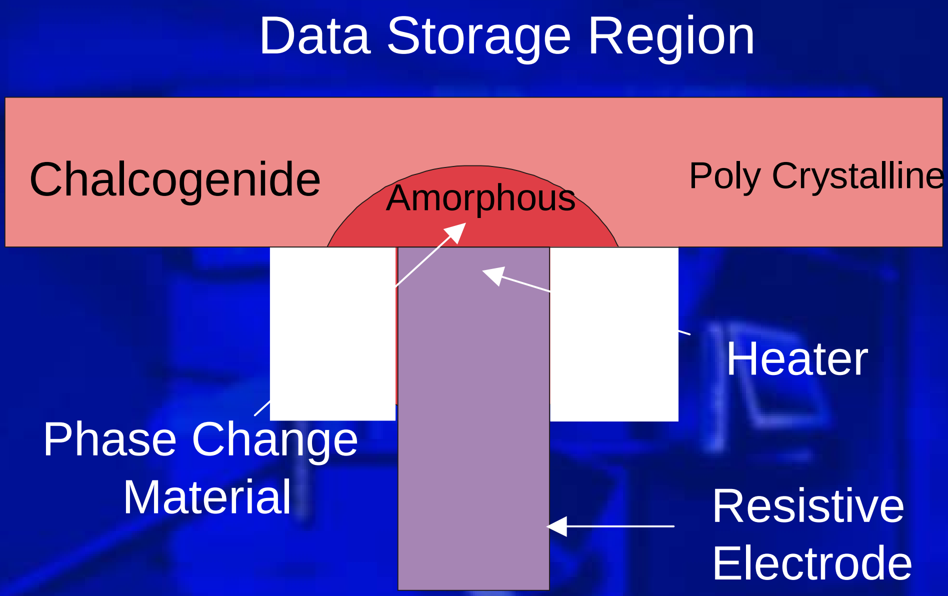
- Tetra/Pentavalent Atom
- Di/Monovalent Metal Atoms
- Oxygen Atoms




$$\vec{E}_{Net} = \vec{E}_{App} - \vec{E}_{Film}$$

# What Is OUM?

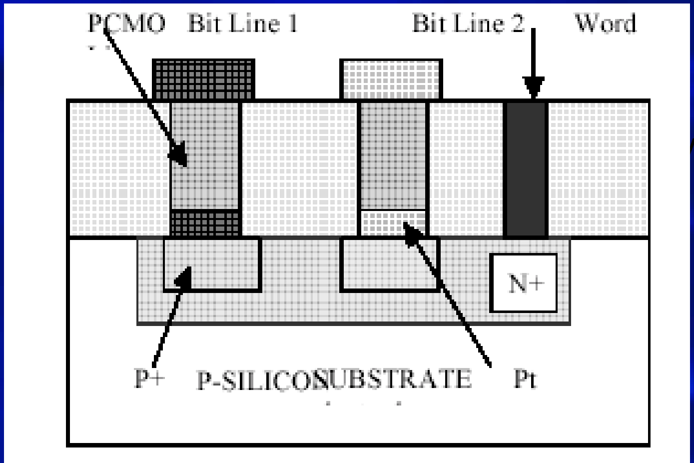
- Operation
  - Chalcogenide material alloys used in re-writable CDs and DVDs
  - Electrical energy (heat) converts the material between crystalline (conductive) and amorphous (resistive) phases
  - Cell reads by measuring resistance




- **Attributes**
  - **Non-volatile**
  - **High density**
  - **Non-destructive read**
  - **Low voltage and low power**
  - **~$10^{12}$ write/erase cycles**
  - **Easy to integrate w/ logic**

# What Is RRAM?

- Operation
  - PCMO material, Complex metal oxide studied for high temp superconductivity
  - Change in resistance with applied electric field
  - Low resistance with forward bias, high resistance when process is reversed
  - Low field read with no charge disturb

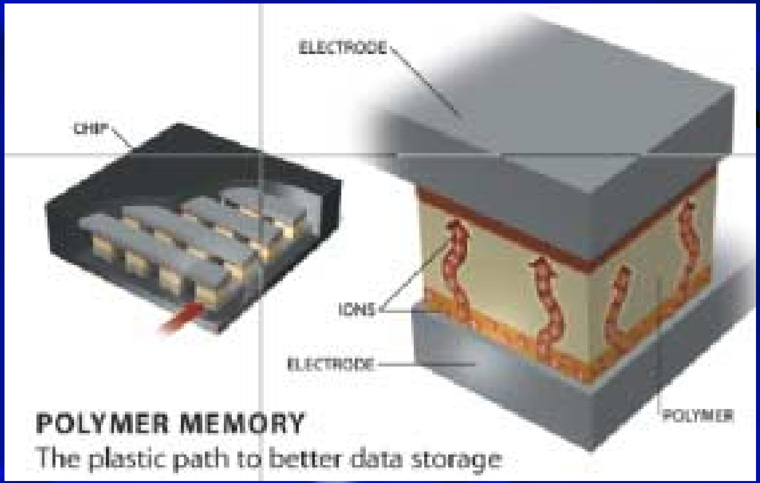



stalline

- **Attributes**
  - **Non-volatile**
  - **High density**
  - **Non-destructive read**
  - **Low voltage and low power**

# What Is Polymer Memory?

- Operation
  - Polymer material with special formulation
  - Change in resistance due to ionic transport with applied electric field
  - Low resistance when ionic conductance paths formed, high resistance when process is reversed when paths broken
  - Low field read with no charge disturb

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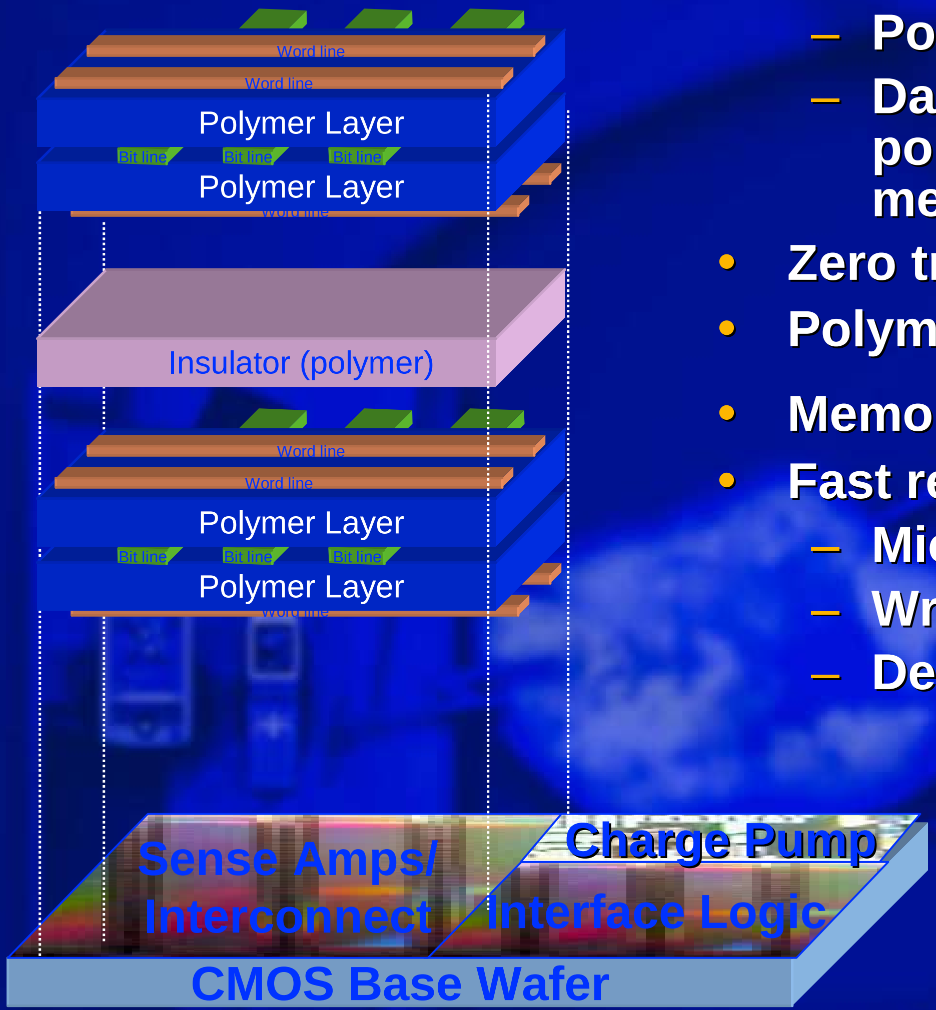
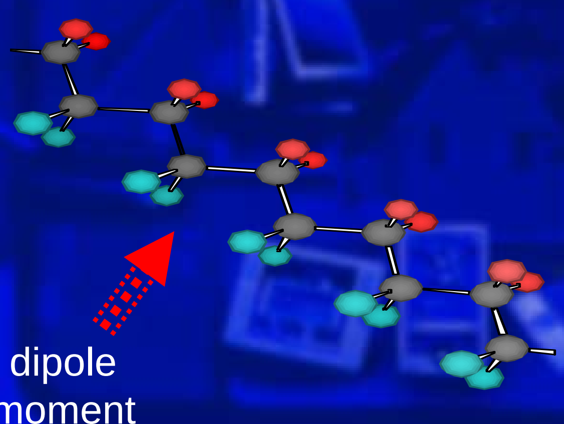
- **Attributes**
  - **Non-volatile**
  - **High density**
  - **Non-destructive read**
  - **Low voltage and low power**
  - **Low cost with polymer**

# What Is Ferroelectric Polymer Memory?




- Polymeric Ferroelectric RAM (PFRAM)
  - Polymer chains with a dipole moment
  - Data stored by changing the polarization of the polymer between metal lines
- Zero transistors per bit of storage
- Polymer layers can be stacked
- Memory is NON-Volatile
- Fast read and write speeds
  - Microsecond initial reads
  - Write speed comparable to flash
  - Destructive read



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# Emerging Non-Volatile Memories

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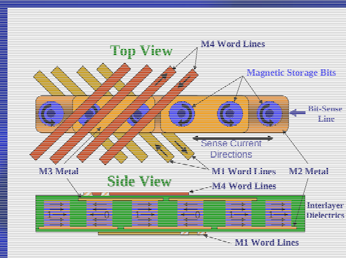


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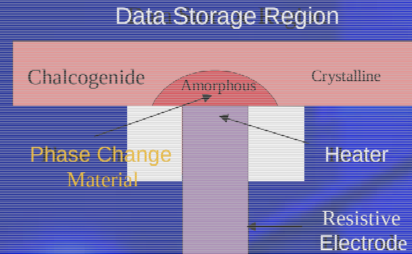


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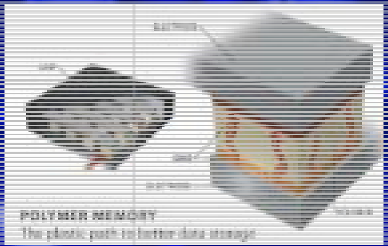


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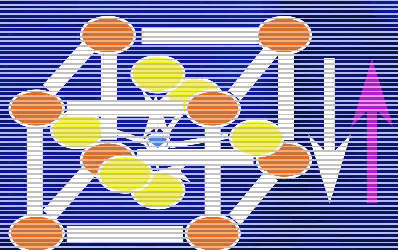

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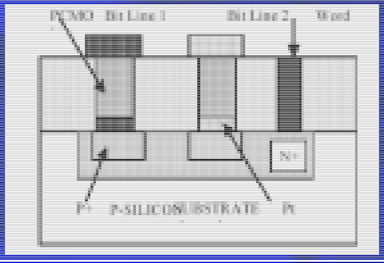


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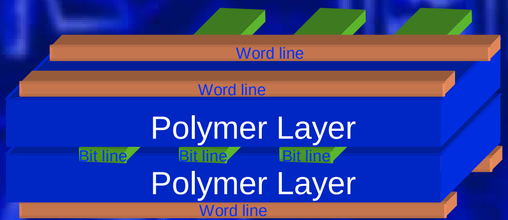


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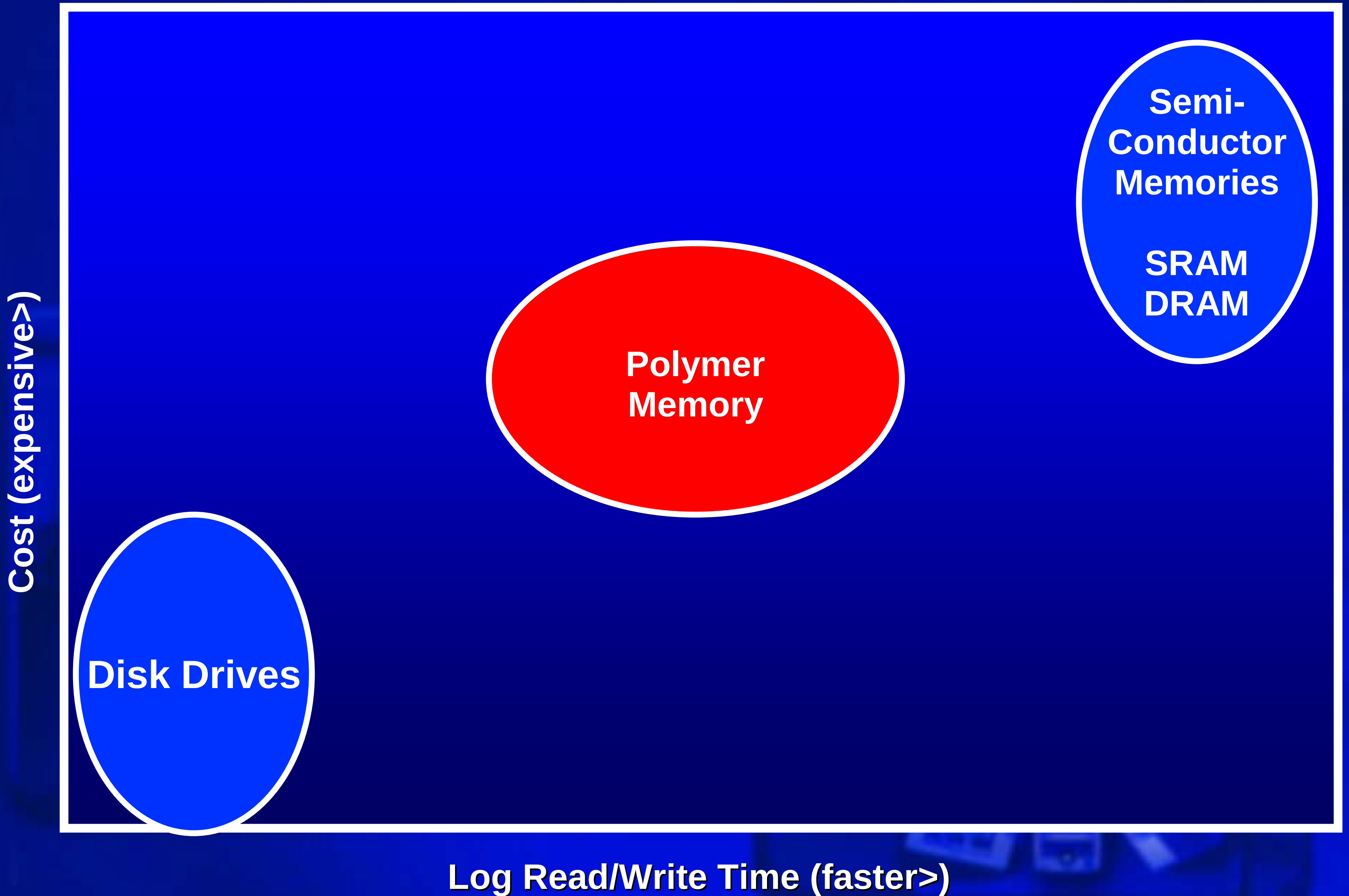
# Value of FE Polymer Memory

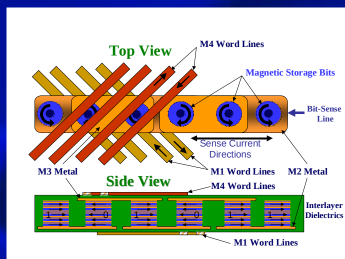


# Value of FE Polymer Memory

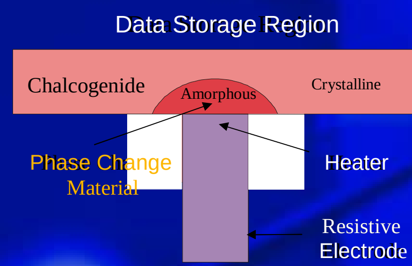
- **Given the relatively slow read and write time (~50 μSec), FE polymer memory is not used for execute in place applications (~100 nSec required)**
- **Instead, it is best used in memory card application where the slower read and write time as well as the $10^8$ cycle capability are adequate**
- **The multi-layer capability can provide very low cost memory systems in portable handheld systems**

# Emerging Non-Volatile Memories

**MRAM**

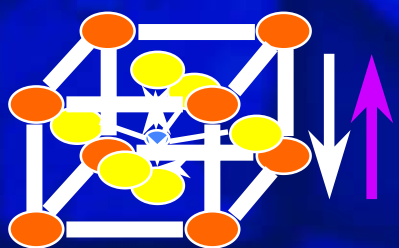



**OUM**

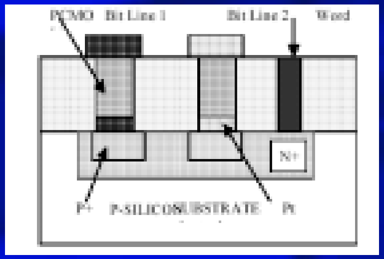



**Polymer**

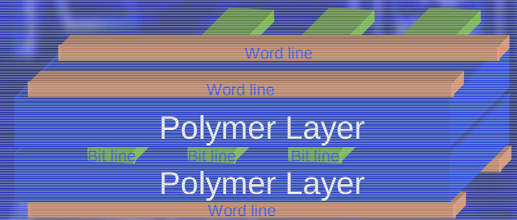

**FERAM**



**RRAM**




**FE Polymer**

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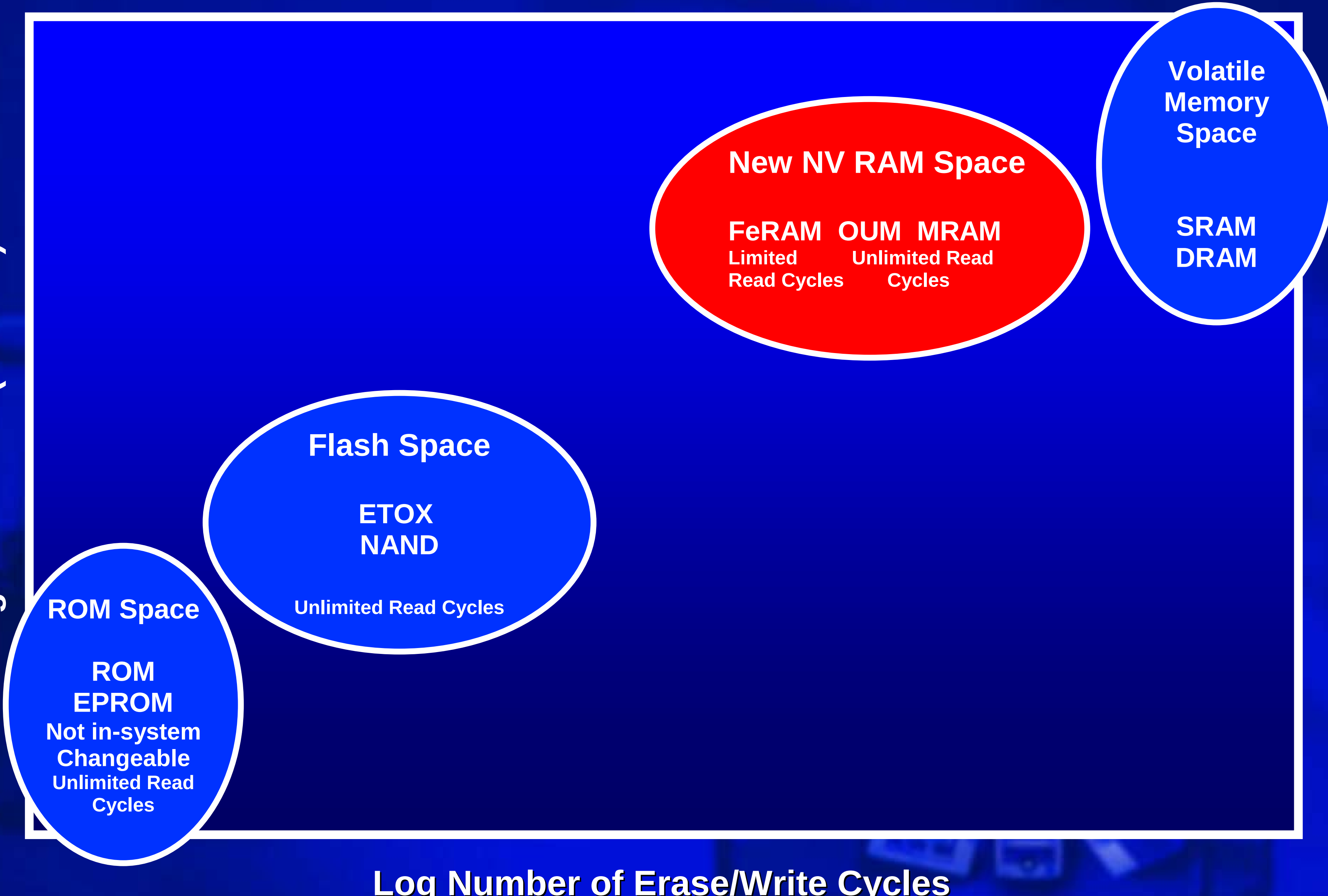
# Value of New NV RAM



# Value of New NV RAM

- Increase in functionality increases market value
- SRAM/DRAMs have fast read/write times and unlimited number of cycles, but they require power to maintain memory
- Flash is non-volatile but is slow to write and limited number of write/erase cycles (1 million)
- A memory that is fast write and capable of high number of write/erase cycles is of high value to low power portable applications
  - Low power is more important than performance: non volatility key
  - Limited cellular bandwidth limits cycle requirement

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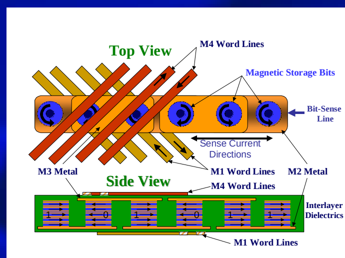


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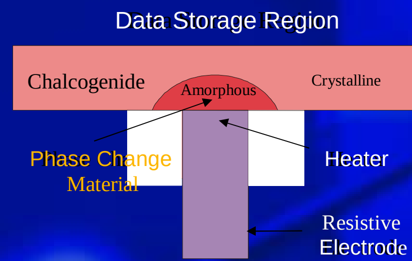
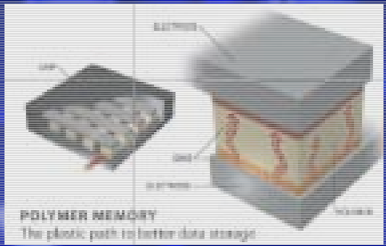



## Ion Polymer

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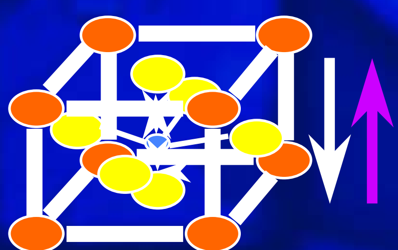

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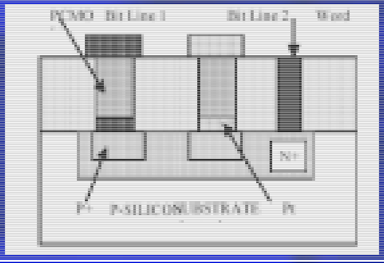

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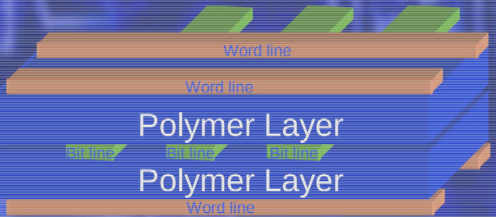


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# Technology Comparison

| MRAM | FeRAM | OUM |
|---|---|---|
| Fastest Read and Write, *Unlimited Cycles* | Fast Read and Write, $10^{12}$ cycles | Fast Read and Write, $10^{12}$ cycles |
| High Current/Power | Lowest Current/Power | High Current/Power |
| Non Destructive Read | Destructive Read | Non Destructive Read |
| Special Process | Special Process | "Bolt on" Process |
| Larger Cell Size | Larger Cell Size | Smaller Cell Size |

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# Unique Challenges of Non-Volatile Memories

- **Commonly accepted NV memory retention time spec is 10 years**
- **Retention is *NEVER* limited by the typical bits: it is always limited by defect mechanisms**
- **Fundamentally, storage mechanisms with fast write may have too low an energy barrier for long term stable retention**
- **In most cases, the write mechanism may cause degradation to either the write mechanism itself or to retention: giving limited cycling capability**

# Circuit Consideration

- All the new memory elements are two terminal devices, acting either as a resistor or a capacitor
  - Different from ETOX® flash, which is a 3 terminal transistor
  - Array architecture important to minimize cross cell disturb
- Ferroelectric devices senses displacement charge from change in polarization: similar to DRAM, low current, but limit to minimum cell capacitance
- MRAM requires sensing of very small change in resistance, most stringent of the new memories
- Resistance change memories all require higher level of switch current from the X-decoder in tight pitch

# Manufacturing Consideration

- All the new memories discussed involves new materials that may not be compatible with standard silicon process and may require new manufacturing processes and new equipment
- Advanced lithography is still required: advancement in lithography including optical enhancement technologies are important for low cost
- With new memory mechanism, new testing methods as well as new testers may be required

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- To maintain Moore's Law cost learning curve, difficult to do it by transistor technology alone
  - New opportunity for new memory structures and new materials
- Current mainstream memory technologies of ETOX and NAND will continue to be the key technologies for more than 5 years out
- Intense research activities to identify scalable memory technologies for 5 year and beyond